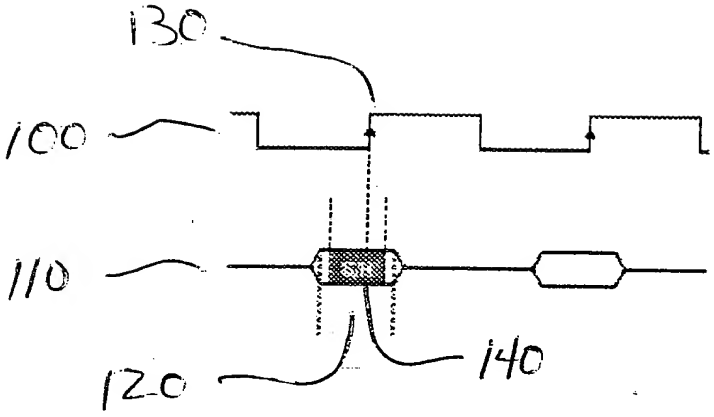
130
100
110
SR
120
140

FIG 1

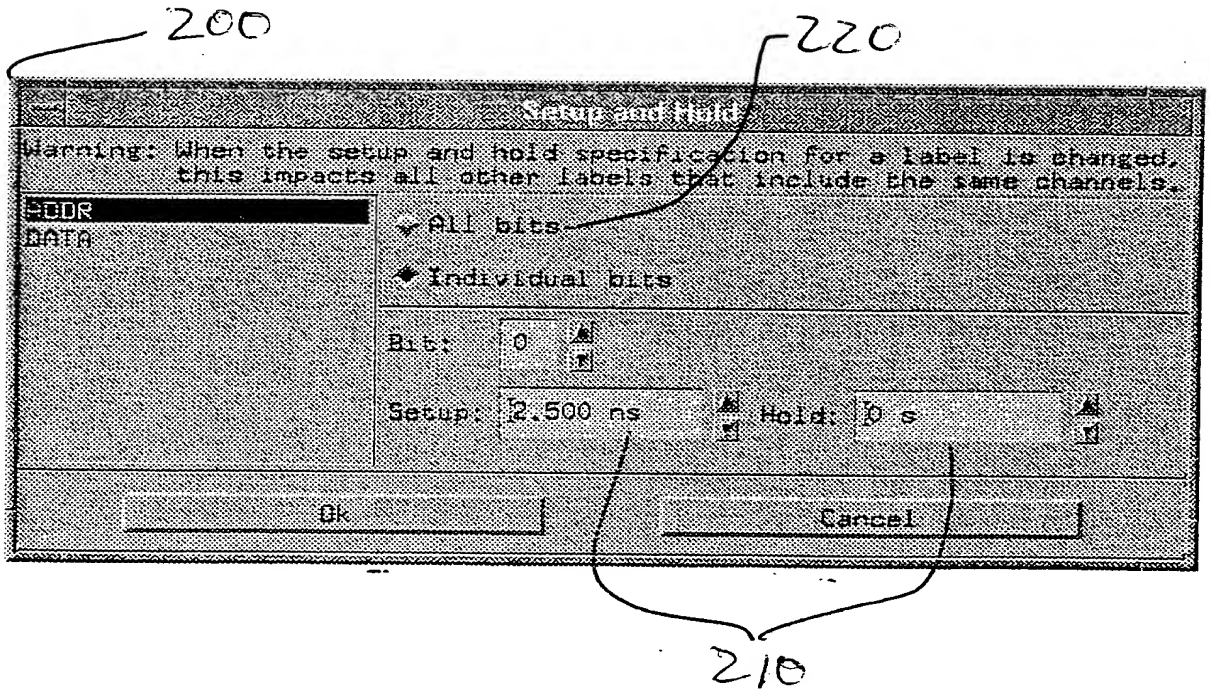
200
220
Setup and Hold
Warning: When the setup and hold specification for a label is changed, this impacts all other labels that include the same channels.
HDDR
DATA
All bits
Individual bits
Bit: 0
Setup: 2.500 ns
Hold: 0 s
Ok
Cancel
210

FIG 2

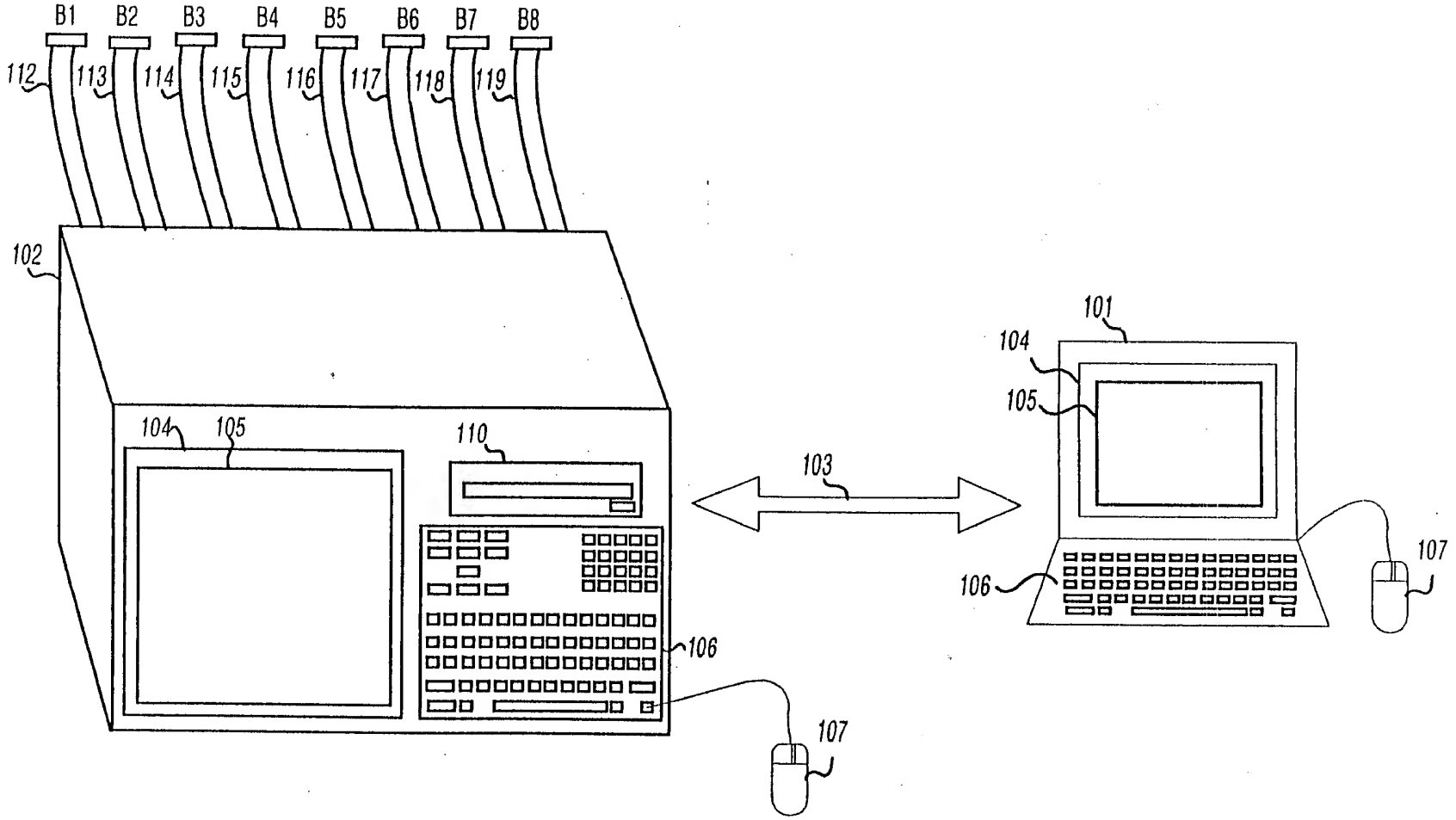

FIG. 3

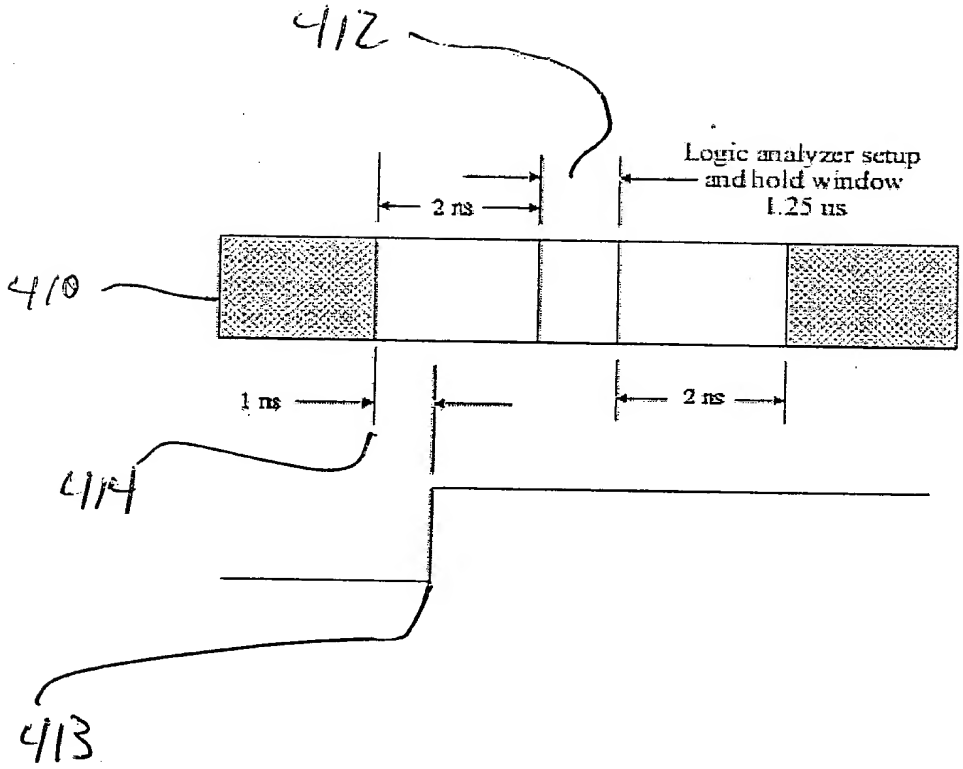
412
Logic analyzer setup
and hold window
1.25 ns
2 ns
410
1 ns
2 ns
414
413

FIG 4

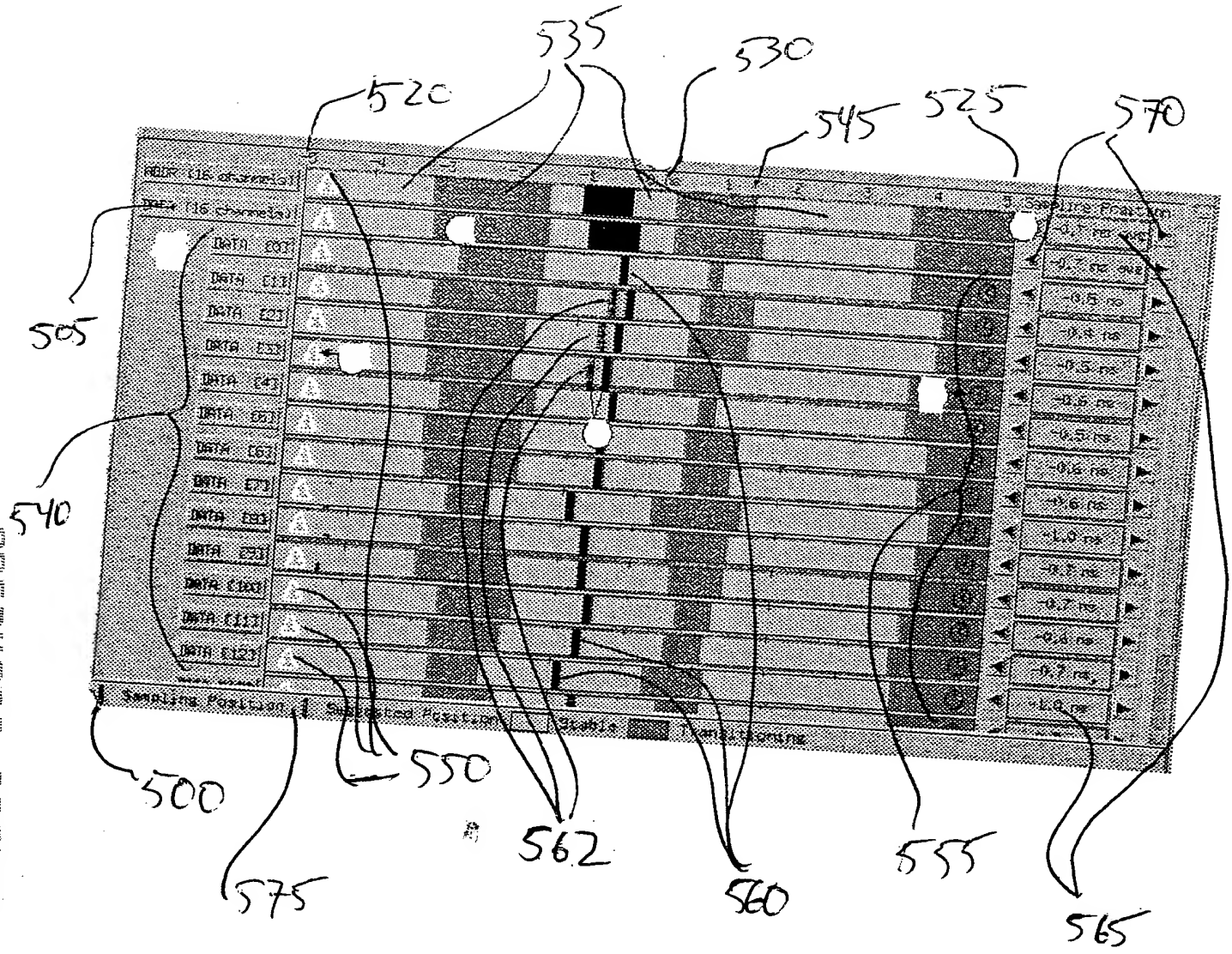
535
530
520
545
525
570
505
540
500
550
562
575
560
555
565

FIG 5

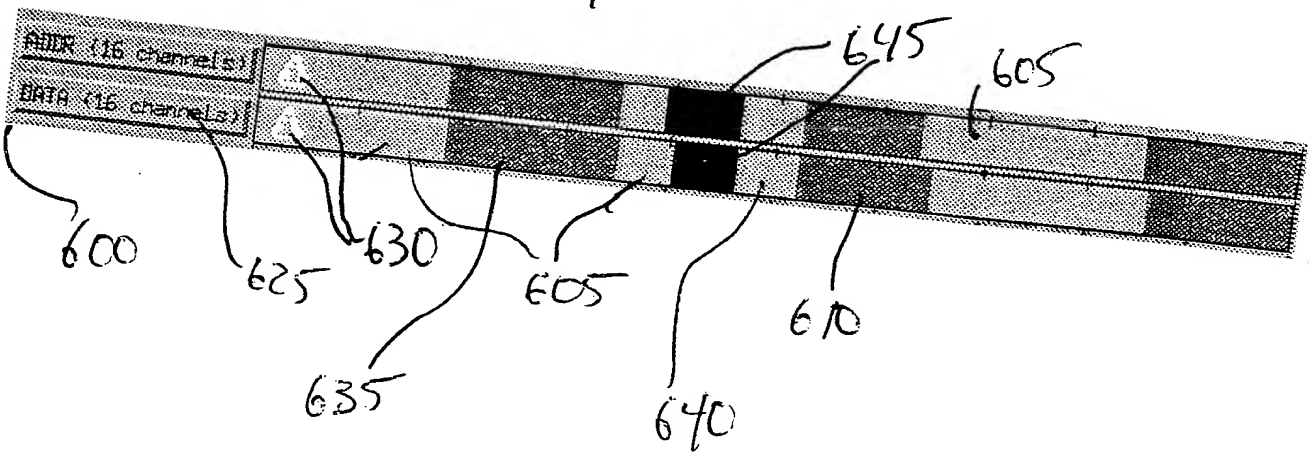
ADDR (16 channels)
DATA (16 channels)
645
605
600
625
630
605
610
635
640

FIG 6

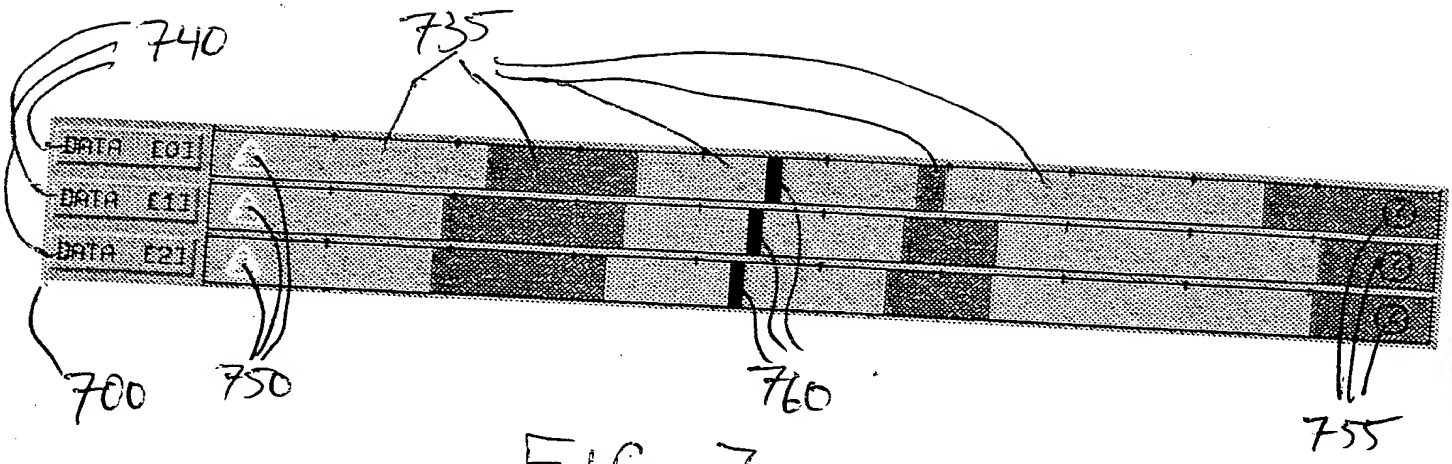

FIG. 7

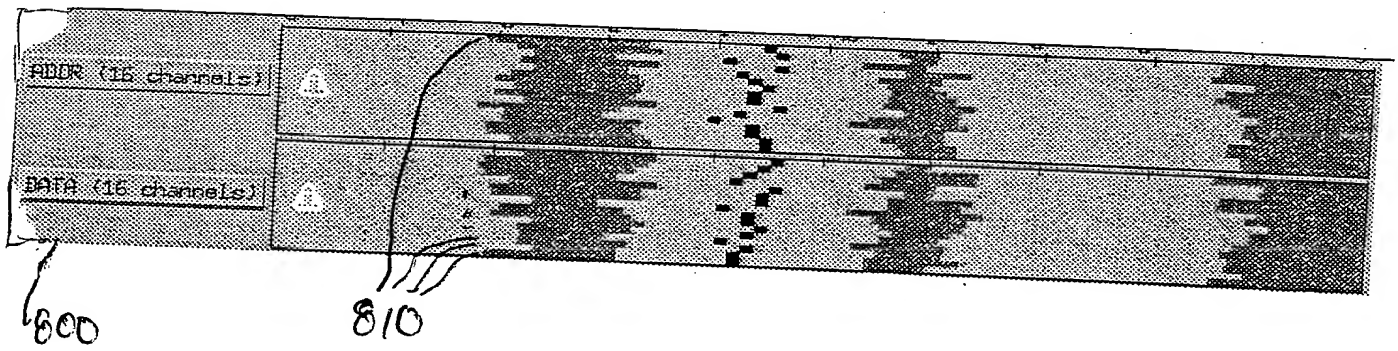

FIG 8

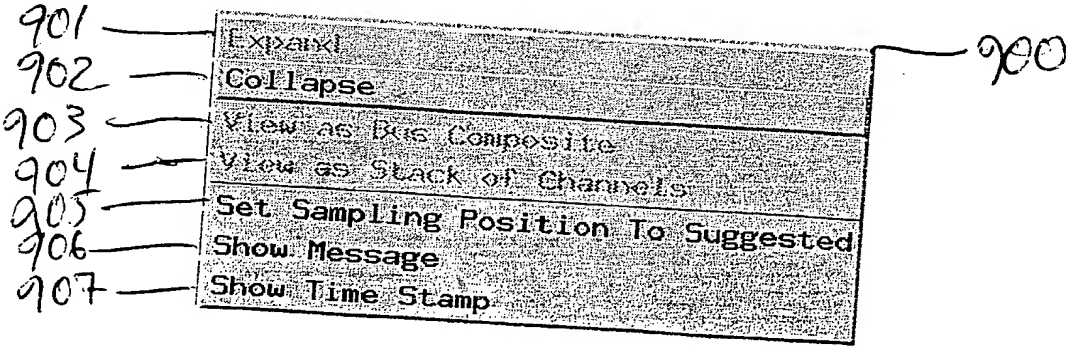

FIG 9

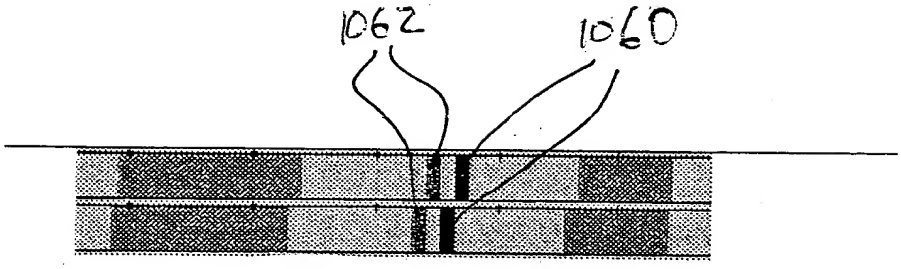

FIG. 10

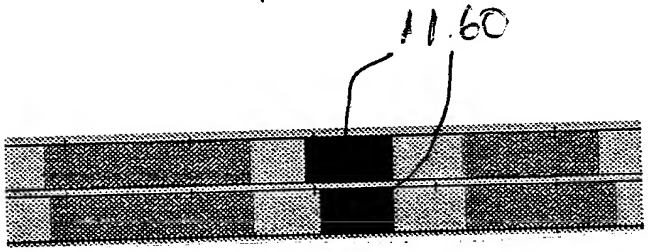

FIG 11

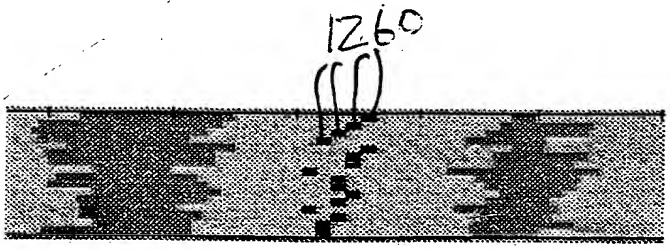

FIG 12